WHAT IS CLAIMED IS:

1. A method of transferring a data bit out of a given cell of an array of memory cells to a latch circuit, comprising the steps of:

selecting a given cell of an array of cells with a first signal;

activating a given SA (sense amplifier), of a plurality of associated SAs, with an enabling second signal to provide a given SA memory cell indicative third signal output;

dynamically NORing a plurality of SA third signal outputs after each one of a series of cyclically occurring pre-charge periods; and

storing and outputting the third signal, in a read latch circuit, for a predetermined interval.

2. A sense amplifier read-out path circuit for high frequency pipelined memory, comprising:

a pair of latch type sense amplifiers defining corresponding respective outputs;

a read latch comprised of NAND logic; and

a clocked switch disposed between the latch and the sense latches receiving the outputs and delivering one of the outputs to the read latch.

3. A method of transferring a data bit out of a given cell of an array of memory cells to a latch circuit, comprising the steps of:

selecting a given cell of an array of cells with a first signal;

activating a given latch type SA (sense amplifier) of a plurality of latch type SAs, the given SA being associated with

said given cell, with an enabling second signal to provide an output signal indicative of the logic value of said given cell;

logically combining the outputs of all of said plurality of latch type SAs to dynamically pass the third signal output of the activated SA after each one of a series of cyclically occurring pre-charge periods; and

receiving and storing the passed third signal, in a read latch circuit, for an output during predetermined interval subsequent to the time of detecting the cell logic value.

4. Apparatus for providing a read-out path for high frequency pipelined memory, comprising:

a plurality of memory cells;

a latch type SA (sense amplifier) connected to each of said plurality of memory cells and operating to sense the logic value of the connected memory cell upon receipt of an enabling signal and subsequently providing an SA output signal indicative of said logic value;

a latch circuit operating to hold a received signal for a predetermined time; and

a dynamic circuit interconnected between each of said latch type SAs and said latch circuit, the dynamic circuit being operable to pass the output signal of the last enabled SA to said latch circuit.

5. Apparatus for providing a read-out path for a plurality of memory cells in a high frequency pipelined memory circuit, comprising:

a plurality of latch type SAs (sense amplifiers) each operable to sense the logic value of a like plurality of memory cells upon receipt of an enabling signal and subsequently providing an SA output signal indicative of said logic value;

a latch output circuit operating to hold a received memory cell logic value indicative signal for a predetermined time; and

a dynamic logic signal passing circuit interconnected between an output of each of said plurality of latch type SAs and said latch output circuit.

6. The apparatus of claim 5, wherein:

the dynamic logic signal passing circuit is a dynamic NOR; and

the latch output circuit is a cross coupled NAND.

7. A method of transferring a data bit out of a given cell of an array of memory cells as a logic value indicative signal to a latch circuit, comprising the steps of:

applying a given memory cell logic value to a sense amplifier (SA) during a pre-charge condition prior to enabling operation of said SA;

enabling said SA to provide an output signal indicative of the logic value of the given memory cell data substantially immediately after enablement; and

passing said output signal to a latch circuit.

8. The method of claim 7, wherein:

the SA holds the logic level of the output for a predetermined time after enablement;

the passing of the signal to a latch circuit is accomplished in a dynamic NOR; and

the latch circuit is operationally a cross-coupled NAND.

9. The method of claim 7, wherein a plurality of memory cells is being read by a like plurality of SAs in consecutive clock cycle time periods and, wherein:

the outputs of each of the plurality of SAs are logically combined in a dynamic manner before passing of the output signal to the latch circuit.

10. The method of claim 7, wherein the SA provides a latching type action of the output signal for a predetermined time after enablement.

11. A method of providing a read-out path for high frequency pipelined memory, comprising the steps of:

sensing the value of a memory cell in a latch type SA (sense amplifier) in a given clock cycle;

holding the sensed value for at least a predetermined time;

transferring the sensed value to a latch circuit; and

outputting the transferred sensed value at a time subsequent to said given clock cycle.

12. Apparatus for providing a read-out path for high frequency pipelined memory, comprising:

a latch type SA (sense amplifier) operable to sense the value of a memory cell in a given clock cycle; and

a latch circuit interconnected to said latch type SA for receiving the sensed value from said SA and outputting the transferred sensed value at a time subsequent to said given clock cycle.

13. The apparatus of claim 12, comprising, in addition:

an additional plurality of latch type SAs for sensing a like plurality of additional memory cells in individually distinct given clock cycles; and

a dynamic logic circuit providing the interconnection between the plurality of SAs and the latch circuit.